|  |
| --- |
|  |
|  |
| ESS DIO CONDITIONING BOARD  Hardware Manual |
|  |
|  |

|  |  |  |
| --- | --- | --- |
|  | **Name** | **Affiliation** |
| **Authors** | Rafael Montaño | RF Group |
| **Reviewers** |  |  |
| **Approver** |  |  |

July 12th, 2016

|  |  |  |  |
| --- | --- | --- | --- |
| **Date** | **Revision** | **Description** | **Authors** |
| 01-Dec-2016 | 0.1 | Initial draft. | Rafael Montaño |
| 29-Dec-2016 | 0.2 | Schematics review of the digital isolation circuits | RF Section |
| 16–Jan-2017 | 0.3 | Files sent for manufacturing | Rafael Montaño |
|  |  |  |  |
|  |  |  |  |

Contents

[1. General information 6](#_Toc472409816)

[1. Introduction 9](#_Toc472409817)

[2. Hardware Characteristics: 9](#_Toc472409818)

[3. Hardware Description 9](#_Toc472409819)

[4. Block diagram 10](#_Toc472409820)

[4.1 Interfaces 10](#_Toc472409821)

[5. Power supply 10](#_Toc472409822)

[**1.1** **Typical Performance Characteristics** 10](#_Toc472409823)

[**1.2** **PCB design** 11](#_Toc472409824)

[2. Manufacturing Specifications 12](#_Toc472409825)

# General information

* **About the document:** This manual is intended to describe the Digital Front-End hardware designed by the ESS RF section team. Information about the hardware configuration, block diagrams, specific schemes, as well as board manufacturing documentation is provided.
* If some part of the text is important it will be noted with the signals that are described in what follows.

**Conventions**

**DANGER**

Indicates that death or severe personal injury will result if proper precaution are not taken.

**Warning**

Indicates that death or severe personal injury may result if proper precautions are not taken.

**Caution**

Indicates that minor personal injury can result if proper precautions are not taken. taken.

**Notice**

Indicates that damage to equipment can result if proper precautions are not taken. taken.

**Information**

**i**

Indicates information that we think you should have read to save your time by avoiding common problems. Important suggestions that should be followed will also be marked with this sign.

* Design reference name: DIO\_COND\_BOARD\_v1
* Manager: Rafael Montaño
* Last production: *Prototype*

CERN Open hardware License v1.2

Through this CERN Open Hardware Licence ("CERN OHL") version 1.2, CERN wishes to provide a tool to foster collaboration and sharing among hardware designers. The CERN OHL is copyright CERN. Anyone is welcome to use the CERN OHL, in unmodified form only, for the distribution of their own Open Hardware designs. Any other right is reserved. Release of hardware designs under the CERN OHL does not constitute an endorsement of the licensor or its designs nor does it imply any involvement by CERN in the development of such designs.

RF Group

European Spallation Source – ESS

Email: [rafael.montano@esss.se](mailto:rafael.montano@esss.se)

**Introduction**

The Digital Front-End interface aims to isolate and protect the I/O module on the FMC – FPGA. The compatible interfaces were defined according to the I/O sensors listed on the signal list.

# Hardware Characteristics:

* 6 Digital inputs isolated and compatible with TTL and 24VDC.
* 4 Digital outputs up to 30VDC, 2 fiber optic output interfaces.
* Internal cable detection
* LED status/interlock indicator

Table 1: Specifications for the Digital Front-end electronics

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Value** | **Comments** |
| Max Input voltage[[1]](#footnote-1) | 30VDC | Input forward current max If = 25mA |
| Input reverse voltage | 5V |  |
| Max Output voltage | 30VDC | Continuous collector or output current 400mA |
| Isolation voltage | 3750 Vrms (min) | Total capacitance (input to output) = 0.8 pF |

# Hardware Description

Six digital inputs selectable between TTL and 24VDC, connected to the DPM1270 through a Molex Triad 48-pins connector, handling TTL input types. Two digital outputs connected through a fiber optic interface isolated from the DPM1270 module.

# Block diagram

The digital Front-End board has the following generic block diagram:



Figure: Block Diagram of the digital Front-End

## Interfaces

The board has the following interfaces:

* Molex Triad 48 connector (74960-3048)
* Fiber-optic:
  + Two fiber optics interfaces to be handle by the FPGA.
* Digital inputs:
  + 6 digital inputs compatible with TTL and 24VDC selectable through a jumper
* Digital outputs:
  + 4 digital outputs transistor open-collector. Pull-up resistor included.
* LEDs:
  + LED status indicator for all DI/O.

# Power supply

The Digital Front-end is powered from the DPM1270 through the MIC2505YM to control the maximum current up to 2A.

* 1. **Typical Performance Characteristics**

*To be tested with the first prototype*

* 1. **PCB design**

Some considerations and comments about the PCB design:

* 2 Layers PCB, digital signals layer and power/ground planes.

Figure: PCB design of the Digital Front-End.

1. **Manufacturing Specifications**

|  |  |  |  |
| --- | --- | --- | --- |
| **Design references** | | | |
| *Name* | DIO\_COND\_BOARD\_v1 |  |  |
| *File name(s)* |  |  |  |
| *Engineer* | Rafael Montaño |  |  |
| *E-mail* | rafael.montano@esss.se |  |  |
| *Fone* | +46-72-179 22 36 | Date | 10 January 2017 |

|  |  |
| --- | --- |
| **Mechanical characteristics** | |
| External size (mm) | 151.4 mm x 369 mm |
| Thickness (mm) | 1.6 mm |
| Multilayers | 2 layers |
| Min track width (mm/mils) | 10 mils |
| Min Hole size (mm/mils) | 15 mils |
| Laminate | FR-4 |
| Pre-preg | FR-4 |
|  | |
| **Finish Copper** | |
| External layers (µm) | 35 µm |
| Holes walls (µm) | 25 µm |
| Internal Layers-Planes (µm) | 35 µm |
| Internal Layers-Signals (µm) | 35 µm |
| **Board finishing requirements** | |
|  |  |
|  |  |
| Silkscreen on top layer (color) | Green |
| Silkscreen on bottom layer (color) | Green |
|  |  |
| Surface Finishing | ENIG – Electroless Nickel / Immersion Gold according to IPC-4552 |
| Thickness | Ni: 3 µm min, 6 µm máx. Au: 0.05 µm min, 0.125 µm máx |
|  |  |

|  |  |
| --- | --- |
| **Additional Information** | |
| Impedance test | No |
| Packaging requirements | No |
| Documentation to be delivered | Manufacturing report |
| Additional control quality requirements | No |

|  |
| --- |
| ***Board Stack up Information*** |
|  |

1. Selectable jumper between TTL and 24VDC, Max. If = 25mA [↑](#footnote-ref-1)